EASA Comment Response Tool

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Title	Regular update of AMC-20
NPA Number	NPA 2020-09

UK CAA (European.Affairs@caa.co.uk) has placed **7** unique comments on this NPA:

Cmt	Segment description	Page	Comment	Attachments
58	AMC 20-158A Aircraft electrical and electronic system high-intensity radiated fields (HIRF) protection — 6. APPROACHES TO COMPLIAN	53 - 64	**Page No:** 63, 78 **Paragraph No:** Figure 1, Figure 3 **Comment:** These Figures seem to be missing some of the step numbers in some of the blocks and some of the arrows do not line up with the blocks. We suggest these should be rectified. **Justification:** Clarity.	
51	AMC 20-158A Aircraft electrical and electronic system high-intensity radiated fields (HIRF) protection — 7. STEPS TO DEMONSTRATE LEVEL A SYSTEM HIRF COMPLIAN	64 - 78	**Page No:** 63, 78 **Paragraph No:** Figure 1, Figure 3 **Comment:** These Figures seem to be missing some of the step numbers in some of the blocks and some of the arrows do not line up with the blocks. We suggest these should be rectified. **Justification:** Clarity.	
52	[AMC 20-193 The Use of Multi-Core Processors] | [AC 20-193 Use of Multi-Core Processors] — 2. APPLICABILI	106 - 108	**Page No:** 107 **Paragraph No:** 2.2.2 **Comment:** The equivalent part of the current EASA MCP CRI requires applicants to contact EASA if they are using this type of technology. It might be helpful for less experienced applicants if a requirement to contact the NAA was added to this document too. It might also be helpful if the note wasn't limited to simultaneous multithreading to limit the potential need for future updates **Justification:** Adding this requirement will ensure that applicants understand the need to discuss the use of implementations such as simultaneous multithreading with their regulator prior to using them. **Proposed Text:** We recommend the following should be added to the end of this paragraph: … "Applicants should inform their regulator if they intend to use simultaneous multithreading, or similar implementations that are not covered by this [AMC]/[AC]".	

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54	[AMC 20-193 The Use of Multi-Core Processors] | [AC 20-193 Use of Multi-Core Processors] — 2. APPLICABILI	106 - 108	**Page No:** 107 **Paragraph No:** 2.3, Bullet 1 **Comment:** The current EASA CRI contains some additional explanatory material related to why MCPs using lock-step mode are exempted. We believe it may help less experienced applicants if this material was included. **Justification:** Adding this explanation would help less experienced applicants understand the reasoning behind this exemption, which will help them with their risk analyses. **Proposed Text:** We recommend the following text should be added as a note: "Lock-step processors with two or more activated cores in which the cores host the same software and execute that same software in lock-step so that their outputs, based on identical input data, can be compared for use in a safety-critical application. (An additional core is sometimes provided for input/output.) These lock-step processors are designed for safety-critical applications and to provide the determinism required, rather than the fast calculations and fast data transfers needed in servers or mobile devices, for which most MCPs are designed. The architectures of lock-step devices do not, therefore, contain features such as shared memory and shared cache that could cause interference. If interference did occur and caused one of the cores to produce a different result from the other(s) or to be delayed in its computations by time interference, these processors are designed to detect differences between the results produced by the cores, so any interference would be detected. The system could then be made safe or could continue to be available if three cores are used with a voting mechanism. For these reasons, this [AMC]/[AC] does not need to apply to lock-step processors that operate in the manner described above."	
55	[AMC 20-193 The Use of Multi-Core Processors] | [AC 20-193 Use of Multi-Core Processors] — 4. DEFINITIO	108 - 110	**Page No:** 108 **Paragraph No:** 4 - Definitions **Comment:** The EASA CRI has a definition of Critical Configuration Settings which is very useful. It would help less experienced applicants if that definition was included. **Justification:** This will help less experienced applicants deal with a critical aspect of MCP management. **Proposed Text:** We recommend a definition of Critical Configuration Settings in the list of definitions should be included, e.g: "Critical Configuration Settings: those configuration settings that the applicant has determined to be necessary for the deterministic execution of the software or any settings that, if inadvertently altered, could change the behaviour of the processor so as to cause the hosted software to no longer comply with its requirements."	

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56	[AMC 20-193 The Use of Multi-Core Processors] | [AC 20-193 Use of Multi-Core Processors] — 5. MULTI-CORE PROCESSOR GUIDAN	110 - 118	**Page No:** 116 **Paragraph No:** 5.4, (1st bullet on page 116) `MCP Platforms with Robust Partitioning' **Comment:** It may be helpful to less experienced applicants to include a note to the effect that: any subsequent modification will need demonstrate that robust partitioning has not been compromised or, if that can't be done, the impact analysis associated with the modification will need to include the additional, target based verification that wasn't performed during the initial approval. **Justification:** This will help less experienced applicants to avoid unexpected increases in the work associated with future modifications. **Proposed Text:** As above.	
57	[AMC 20-193 The Use of Multi-Core Processors] | [AC 20-193 Use of Multi-Core Processors] — 5. MULTI-CORE PROCESSOR GUIDAN	110 - 118	**Page No:** 118 **Paragraph No:** 5.7, MCP Objectives Table – MCP Objective "**MCP_Resource_Usage_2"** **Comment:** There is a typographical error in the "IDAL A or B" Column. It currently reads "n/a", we believe it should read "Yes". **Justification:** Correction of objective applicability. **Proposed Text:** Amend "n/a" to read "Yes".	